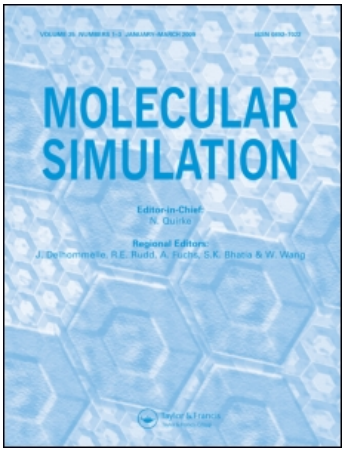

Molecular Simulation
Publication details, including instructions for authors and subscription information:
http://www.informaworld.com/smpp/title~content=t713644482

Topography simulation for structural analysis using cell advancing method

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To cite this Article Lee, J. -G. , Yoon, S. and Won, T.(2005) 'Topography simulation for structural analysis using cell advancing method', Molecular Simulation, 31: 12, 851 — 857
To link to this Article: DOI: 10.1080/08927020500259859
URL: http://dx.doi.org/10.1080/08927020500259859

Molecular Simulation, Vol. 31, No. 12, 15 October 2005, 851–857

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Topography simulation for structural analysis using cell advancing method2

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(Received June 2005; in final form July 2005)

In this paper, we propose a novel method for topography simulation in micro-electronic processes such as deposition and etching processes. The proposed scheme comprises of calculating the forward and backward movement of the surface and converting the cell structure into a tetrahedral mesh structure with topological information. Memory requirements are mitigated through a dynamic allocating scheme, which takes only the surface cells under consideration. For the removal of cells, a fixed time step is employed while volume remains in the surface cells. A spillover algorithm has also been devised in order to consider the case when more volume has to be removed from a cell during a single time step. Our proposed scheme was applied to the cases such as the construction of a TFT-LCD structure, ROM and a DRAM cell. A numerical simulator was interfaced with the topography simulator in order to investigate the successful meshing operation form the cell structure. For exemplary application, parasitic capacitances were extracted from a test wafer structure having 4 metal lines embedded in two types of non-planar dielectric layer. The simulation result exhibited about maximum 8% error, which seems to be relatively small in comparison to the planar dielectric layer.

Keywords: Topography simulation; Deposition; Etching; Cell advancing method; Mesh generation

1. Introduction

Full three-dimensional (3-D) topography simulation is an important tool for investing the complex structure in sub-micrometer semiconductor processing. Much needed research has been undertaken to develop novel schemes, which allow designers to figure out the topographical evolution of the surface during front-end semiconductor processes such as deposition and etching. Exact understanding of topographical evolution is especially important for optimizing the front-end process in nanometer semiconductor process. Despite many research efforts have been made on the development of novel schemes, three-dimensional topography simulation is still faced with many challenges, which limit the general applicability and usefulness.

A variety of surface evolution methods have been studied for three-dimensional topography simulators; the string method, the level set method and the cell method [1–8]. The completed simulators have been used to investigate various three dimensional topography. The conventional string method sometimes causes fatal errors such as the looping of strings. The loops arise naturally at slowly etching convex corners with fast etching sides. The level set method offers quite an accurate profile for tracking interfaces despite of its inherent issue of computationally inefficiency. Furthermore, the traditional cell method has a limit because it requires intensive memory. However, the cell method has a unique feature such as the capability to easily handle the topographical evolution, adaptive meshing scheme and relatively simplicity for the extension to the three-dimension. In this paper, we propose a cell advancing method, which is different from the traditional cell method for topography simulation. Using the finite element method (FEM), we perform a mesh generation of the simulated topography for the calculation of parasitic capacitances.

2. Simulation method

2.1 Topography simulation method

The proposed topography simulation method easily handles arbitrarily shaped geometries. The cell structure is generated according to the following procedure.

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Molecular Simulation
ISSN 0892-7022 print/ISSN 1029-0435 online © 2005 Taylor & Francis
http://www.tandf.co.uk/journals
DOI: 10.1080/08927020500259859

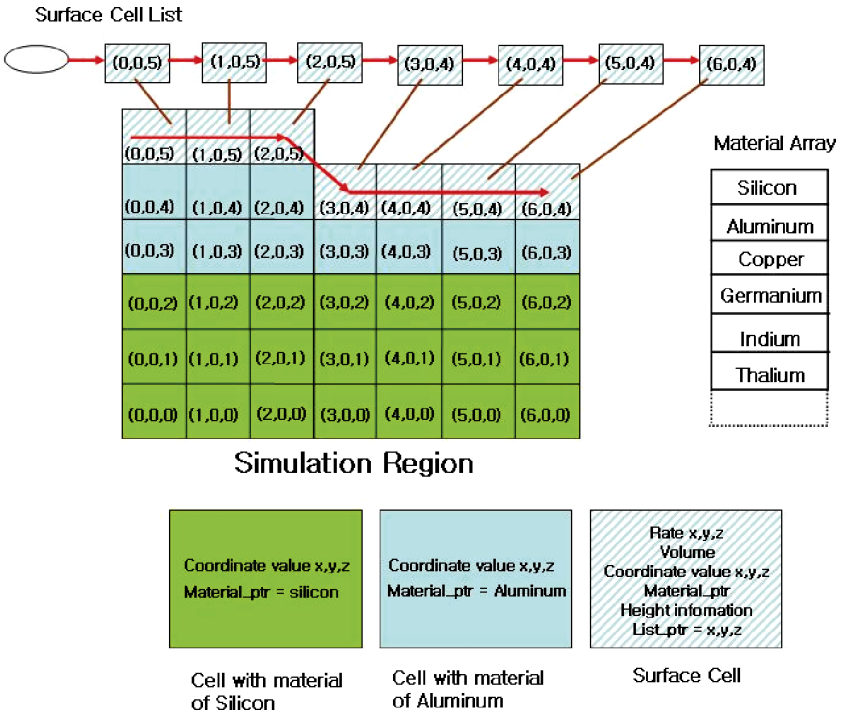

Figure 1. Simulator topography data allocation scheme.

The simulation region is divided into units of hexahedron-shaped cells. Both material information and coordinate value are assigned at each divided cell. The cells exposed to the vacuum are defined surface cells. The surface cells are constituted as the list cells for efficiency use of memory. Only the exposure information, etch/deposition rate and cell volume are assigned at surface cells as shown in figure 1. To generate mesh structure, the height information is assigned at surface cells.

The surface evolution traces the forward and backward movement of surface through a list structure, so called the surface cell list. The surface movement allows arbitrary change of actual geometry in accordance with recalculated rate distribution, which supports quite a complex structure.

After the dividing of the units of hexahedron-shaped cells, the surface cells are constructed linked list structure. Figure 2 is a schematic diagram illustrating the present method wherein the list constitutes a surface cell. Figure 2(a) is a schematic diagram illustrating the composition of the surface cell list for a surface topography expression for the case of etching. The surface cell list is composed of cells exposed to the vacuum (List1). Figure 2(b) is a schematic diagram illustrating the composition of the surface cell list for a surface topography expression in the case of deposition. The surface cell list is composed of vacuum cells exposed to the surface (List2). The surface cell list is used to perform the simulation for forward and backward movement of the surface.

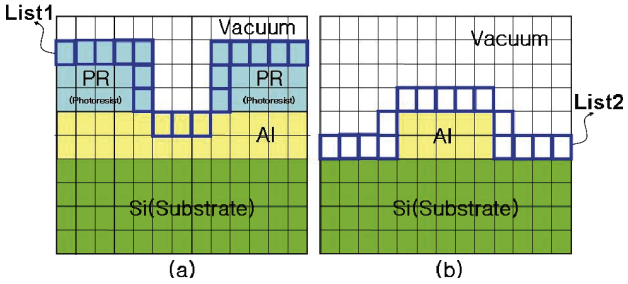

Figure 2. The cell list composition for a surface topography expression (a) the case of etching, (b) the case of deposition.

Cells are removed one by one according to the local etch rate while a number of cells are exposed to the etching medium. During the deposition process, a cell is added one by one in accordance with a local deposition rate while the cell faces are exposed to the deposition medium.

The surface cell is removed according to the following procedure as shown figure 3. At single time step, the list of surface cell is searched. The number of exposed cell faces is counted. The removed cell volume is calculated according to equation (1) in one time step. If the cell volume removed totally, then that surface cell is removed from the list. The time step Δt is updated. The variable describing the cell volume that has been removed is updated at the same time. Finally, newly exposed cell is added surface cell list, before the next time step may begin. The surface cells are removed until time T is reached. Time (T) is defined according to the user's selection.

Calculating the volume removed in one time step is expressed as

$$\text{removed volume} = \frac{(R \times \Delta t) \times S}{V_{\text{total}}} \qquad (1)$$

where R is the total etch rate or deposition rate of the cell. The cells are cubic that their side length (dx, dy and dz) are unity. V_{total} is total volume ($V_{\text{total}} = dx \cdot dy \cdot dz$). The

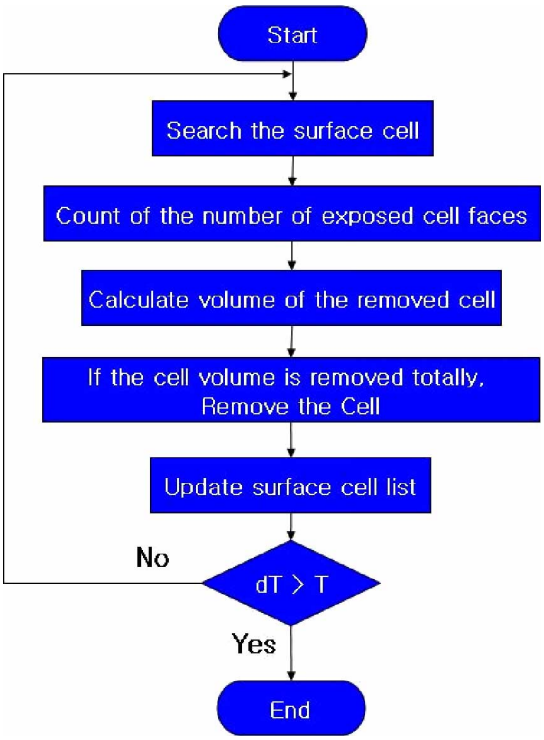

Figure 3. The flowchart of the cell removal.

Δt is time step. The area S is face exposed to the developer.

The exposed cell face is derived as follows for each condition of the cells. If a single face of a surface cell is exposed, then the area of exposed face is given as

$$S = \mathrm{d}x \cdot \mathrm{d}y \tag{2}$$

If two neighboring faces (for example x-y and y-z planes) of a cell are exposed, the development is accelerated as follows, and then the area of exposed face is given as

$$S = [(\mathrm{d}x^2 + \mathrm{d}y^2)^{1/2}] \cdot \mathrm{d}y \tag{3}$$

If the neighboring three faces (for example x-y, y-z and x-y planes) are exposed, then the area of exposed face is given as

$$S = [(\mathrm{d}x \cdot \mathrm{d}y)^2(\mathrm{d}y \cdot \mathrm{d}z)^2 + (\mathrm{d}x \cdot \mathrm{d}z)^2]^{1/2} \tag{4}$$

For etching and deposition processes consider information surface reactions to calculate etch or deposition rated along the exposed surface. Since a variety of process models for etching and deposition, the quantities such as etch or deposition rates are measurable in semiconductor technology [9–11]. We use following equation (5) to calculate etch or deposition rate.

The removed volume of surface cell are calculated by the total etch rate or deposition rate. Total etch rate or deposition rate is expressed as

$$(R_x \cdot V_x + R_y \cdot V_y + R_z \cdot V_z)I(x, y, z) \tag{5}$$

where R_x, R_y and R_z are the etch rate or deposition rate of x, y and z axis direction. Here, V_x, V_y and V_z are the visibility along the x, y and z axis direction. $I(x, y, z)$ is the quantity of incident particle at the location of the surface cell.

Since topography processes are much influenced by the shape of the surface, topography simulator should employ information about the incident particle distribution and the exposure information of surface. To determine the distributions of incoming particles are used the resulting particle flux distributions at a surface point. The region beyond the surface is divided into several patches in a spherical coordinate system with a polar angle Θ and azimuth angle ϕ as shown in figure 4.

The incident flux is the integrated over those patches of the hemisphere, which are visible from the surface point. If a surface patch is visible from a point on the surface, visibility has to be performed along a given direction.

The visibility expresses the exposure information of the cell about the direction for evolution. Figure 5 illustrates the scheme for calculating the change of visibility in accordance with the location of each cell. The C1 cell has a visibility of a factor of two when compared with the C2 cell along the x-axis and z-axis directions. The C2 cell has an additional visibility due to reflection.

When, during etch simulation, the decrement amount exceeds the volume of a surface cell, the decrement is delivered to the next volume. Erroneous calculation can be performed in case when more volume is cleared than needed in a fixed time interval. We devised a spillover

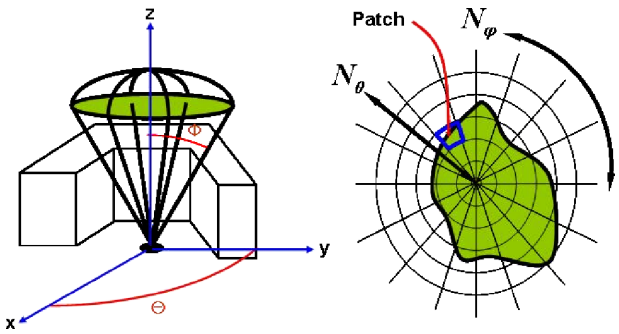

Figure 4. A top view of the hemisphere above the analysis region.

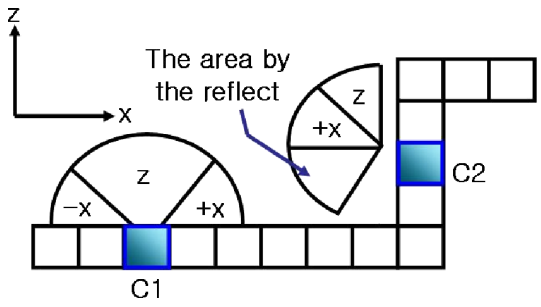

Figure 5. The change of visibility according to the location of the cell.

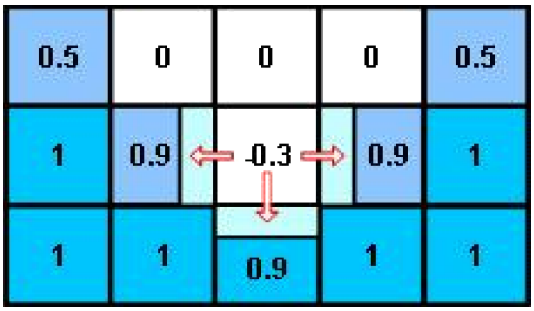

Figure 6. Basic scheme of the spillover algorithm concept.

algorithm to resolve the problem. The spillover algorithm is to remove a partial volume of adjacent cell to take into account the over-etched volume.

If for example, the volume value of a given cell is 1 and the decrement is 0.3. After each time step the resulting volume value of removed cells is distributed to adjacent cells in the same direction during the etch simulation. Figure 6 shows a basic scheme of the spillover algorithm under this work.

2.2 Mesh generation method

The final structure was used for the generation of layered meshes. The cell structure was converted into a tetrahedral mesh structure with topological information. Figure 7 is a schematic diagram illustrating the mesh generation.

The generated cell structure is converted with tetrahedral mesh structure according to the following procedure. Firstly, we acquire the height information with each cell from cell structure of the topography as shown in figure 7(a). The numeric character is the height information (see figure 7(a)). Secondly, each cell is combined with cells of same height information. Figure 7(b) shows the combined cells information. The combined cell information is formed to combine the cell of the same height information. Thirdly, to generate mesh of the non-planer surface, we need height information and boundary information of equivalent cells about the node point P as shown in figure 7(c). And lastly, it is generated the tetrahedral mesh structure as shown in figure 7(d).

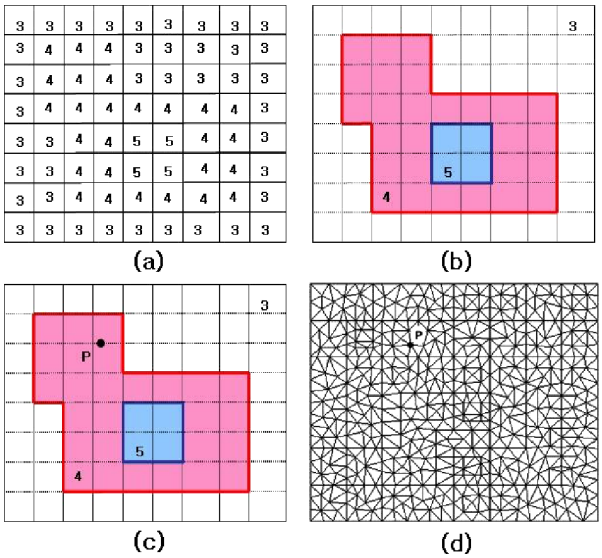

Figure 7. The method of mesh generation (a), (b) and (c) cell height information and boundary information of equivalent cells (d) tetrahedral mesh generation.

3. Result and discussions

In this section, we show a series of results using the above cell advancing methods. Several topography simulation results demonstrate the proposed cell advancing method is quite efficient for application. The developed topography simulator was interfaced with a numerical simulator in order to investigate the successful meshing operation from the cell structure.

3.1 Extract parasitic capacitance

Figure 8 is shown an example for testing the validity of the proposed scheme. The test structure has 4 metal lines, which are embedded with two types of non-planar dielectric layer.

The test structure is the one which the paralleled metal lines intersects each other. The lower part metal line is embedded in the dielectric layer. The final upper part metal line has the non-planar surface as shown in figure 8(a) and (b). Also, the upper part metal line is embedded in the dielectric layer. The lower part metal line has a non-planar surface as shown in figure 8(c) and (d).

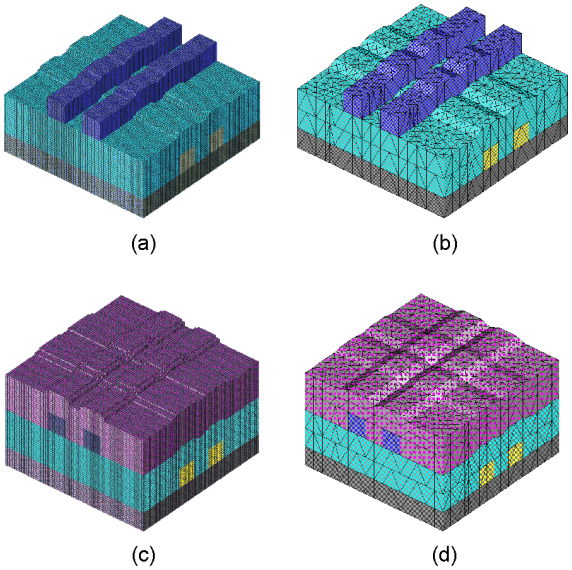

Figure 8. The case of the 2 metal lines embedded one types of non-planar dielectric layer (a) cell structure, (b) the result of a mesh generation. The case of the 2 metal lines embedded two types of non-planar dielectric layer (c) cell structure, (d) the result of a mesh generation.

Table 1. The table shows parasitic capacitance values of the case which the non-planar is considered and not considered.

	Parasitic capacitance value (pF)
The case which the winding by the wiring is considered	$\begin{bmatrix} 1.513 & -0.388 & -0.194 & -0.193 \\ -0.398 & 1.518 & -0.194 & -0.194 \\ -0.194 & -0.194 & -0.505 & -0.384 \\ -0.193 & -0.194 & -0.384 & -1.504 \end{bmatrix} \times 10^{-3}$
The case which the winding by the wiring is not considered	$\begin{bmatrix} 1.491 & -0.397 & -0.178 & -0.178 \\ -0.317 & 1.491 & -0.178 & -0.178 \\ -0.178 & -0.178 & 1.491 & -0.178 \\ -0.178 & -0.178 & -0.403 & 1.472 \end{bmatrix} \times 10^{-3}$

Using the mesh information, the parasitic capacitances are calculated between the metal lines. The parasitic capacitance is expressed as

$$C = \begin{bmatrix} \sum C_{1j} & -C_{12} & \cdot & \cdot & -C_{1N} \\ -C_{12} & \sum C_{2j} & \cdot & \cdot & -C_{2N} \\ \cdot & \cdot & \cdot & & \cdot \\ \cdot & \cdot & & \cdot & \cdot \\ -C_{N1} & -C_{N2} & \cdot & \cdot & \sum_{j=1}^{N} C_{Nj} \end{bmatrix} \quad (6)$$

The diagonal elements in ii^{th} are the total parasitic capacitance. The total parasitic capacitance is expressed as the sum of the coupling capacitance of line in i^{th}, parasitic capacitance (C_{ii}) between ground and other lines. The elements in the ij^{th} express parasitic capacitance between i^{th} line and j^{th} line.

This table provides the calculated parasitic capacitance values for the two cases wherein the non-planar is considered and not considered (see table 1). The calculated value is a parasitic capacitance where the parallel metal lines intersect each other. The simulation result exhibited about 8% maximum error, which seems to be relatively small in comparison to the one of the planar dielectric layer. The change of such parasitic capacitance is altered according to the form of the non-planar. The influence about the non-planar must consider consequently.

3.2 ROM structure

As a first example, figure 9 shows three-dimensional topography simulation of a ROM structure. This resulting is a final profile structure on the wafer after topography simulation in accordance with the user-defined layout and process procedure.

According to the proposed cell advancing method, simulation region is divided into units of hexahedron-shaped cells. The simulation region is used the size 452 × 156 × 8 μm. This structure has total 426,400 (104 × 50 × 82) cells. The memory of this structure is used physical RAM of 8.352 Mbyte from using the proposed method. The generated structure converts triangle mesh structure to calculate the parasitic capacitance. To calculate the parasitic capacitance must be considered the influence by the non-planar. This ROM structure has many non-planar as shown in figure 9. This structure takes the influence by the non-planar much more. Consequently the structure must consider the form of the non-planar.

3.3 DRAM cell structure

Our proposed scheme was applied to the cases such as the construction of a DRAM cell. The generated structure has 4 cell capacitors which are the paralleled each other. And the structure is constructed bit line, word line, the lower part of the electrode and the higher part of the electrode. This resulting is a final profile structure on the wafer after topography simulation in accordance with the user-defined layout and process procedure.

Figure 10 shows the simulation result for a DRAM cell structure. The simulation region occupies a dimension of 2.25 × 1.75 × 3.45 μm. This structure has total 1,611,792 (104 × 82 × 189) cells. The physical RAM was required a size of 32.5 Mbytes.

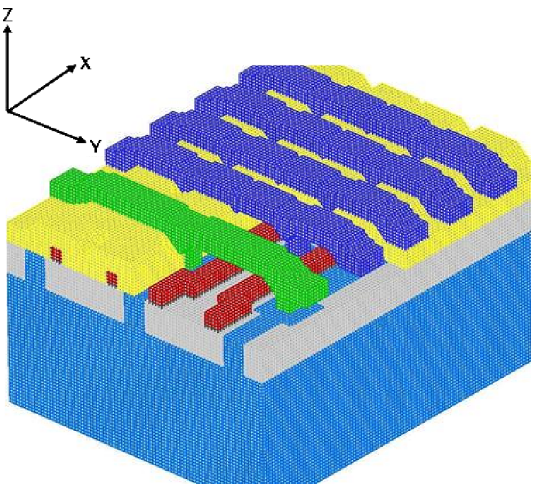

Figure 9. The result of topography simulation of a ROM structure.

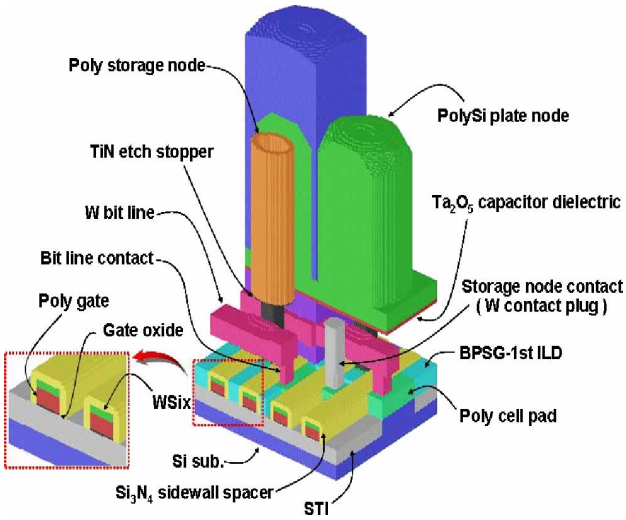

Figure 10. The result of topography simulation for the DRAM cell structure.

The DRAM cell is converted mesh structure from the cell structure as shown figure 11. This resulting demonstrates the successful meshing operation from the complex cell structure of figure 10.

3.4 TFT-LCD structure

Figure 13 shows the simulation result for the PVA structure of TFT-LCD. This resulting is simulated with the proposed cell advancing method. This resulting is a final profile structure after topography simulation in accordance with the user-defined layout and process procedure. The user-defined layout is shown as figure 12.

The liquid crystal cell is taken the influence of the characteristic of non-planar. Therefore the liquid crystal cell must consider about the characteristic, which appears consequently in the non-planar. But the case of the TFT-LCD has about 270 × 90 μm which is the ranges to *XY* plane. The thickness of the top and bottom is approximately 6 μm including the liquid crystal and electrode. Especially, the thickness of the electrode is less than 0.1 μm. Therefore the non-planar must consider about the case of the 0.1 μm which is the thickness. If the minimum cell size is assumed 0.1 μm. The number of cells is 2700 × 900 × 60. The resulting memory is need not more than 500Mbyte to store the information of the cells. The memory is desired efficient management method. But our proposed method guarantees computational efficiency with affordable memory size due to efficiency in implementing the cell list. The memory of this structure is used physical RAM of 97.352Mbyte from using the proposed method.

4. Conclusion

In conclusion, we report a novel topography simulation scheme for numerical analysis of complex device structure. The developed topography simulator was interfaced with a numerical simulator in order to investigate the successful meshing operation from the cell structure. The proposed method guarantees computational efficiency with affordable memory size due to efficiency in implementing the cell list. The proposed scheme was employed for the calculation of parasitic capacitance values of a test structure having 4 metal lines embedded with two types of non-planar dielectric layer. The simulation result exhibited approximately 8% maximum error compared to that of planar dielectric layers. Several topography simulation results demonstrate the proposed cell advancing method is quite efficient for application. Our proposed scheme was applied to the cases such as the construction of a DRAM cell, TFT-LCD structure and ROM structure. It is considered that the cell advancing method is very suitable to figure out the profile during the deposition/etching process of nano-scale processes.

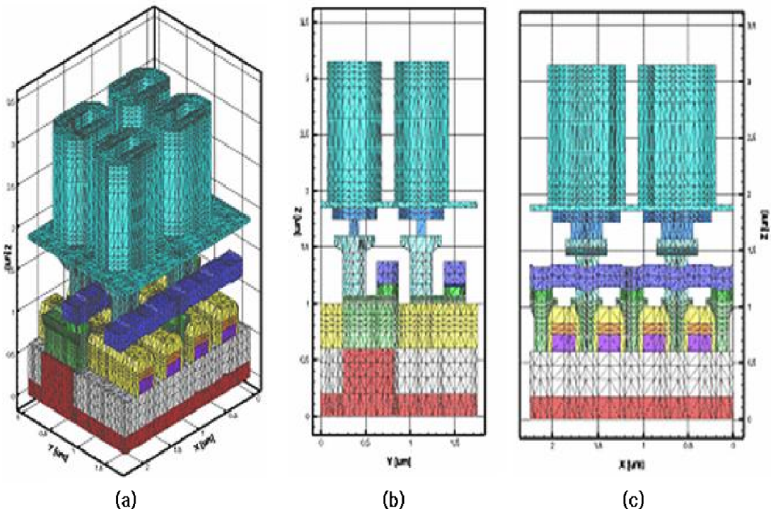

Figure 11. Results of generation for DRAM cell structure: (a) Bird-eye's view, (b) Side view of word line direction, (c) Side view of bit line direction.

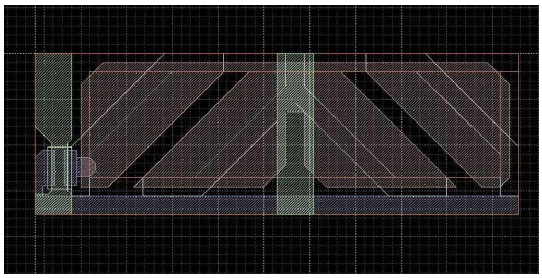

Figure 12. The layout of PVA mode liquid crystal cell.

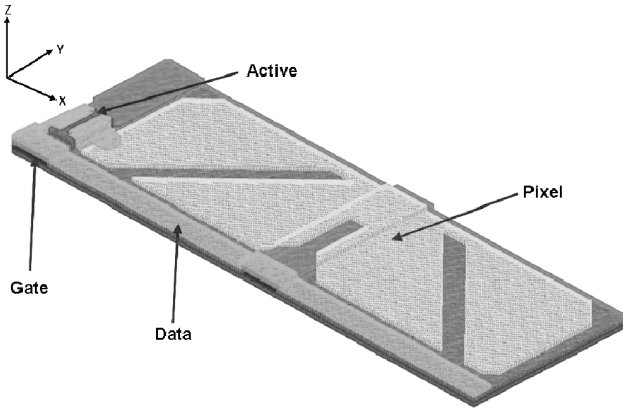

Figure 13. The result of topography simulation of a PVA mode liquid crystal cell.

Acknowledgements

This work was supported partly by the Korean Ministry of Information & Communication (MIC) through the Information Technology Research Center (ITRC) Program supervised by IITA, and partly by the Korean Ministry of Science and Technology (MOST) through the Tera-Nano Development (TND) Program and the Nano Core Basic Research Program (M1-0213-04-0002) by KISTEP.

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